KOYEL GHOSH

STREAM-IT 3rd SEM

Roll No.-16500221044

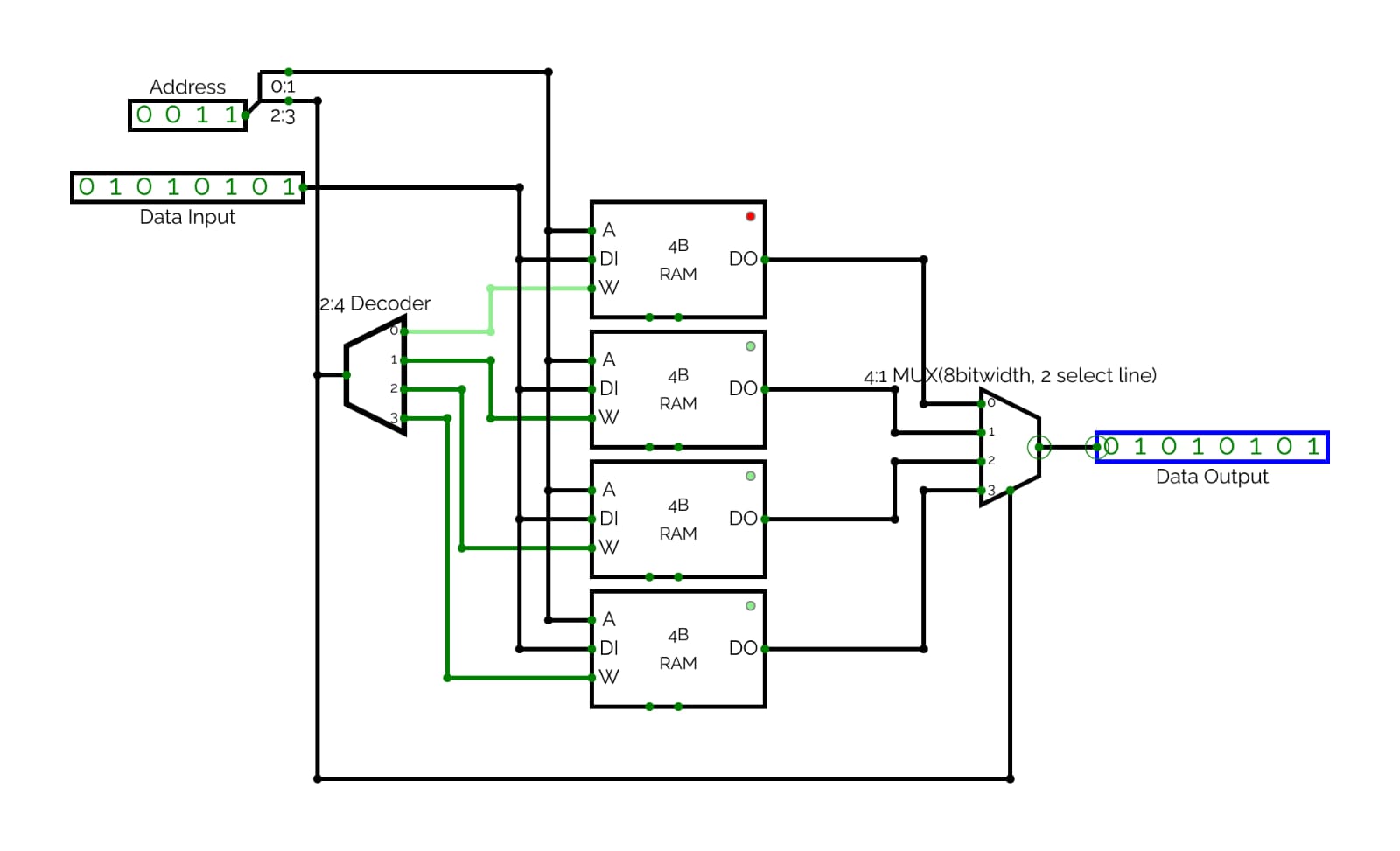
Subject Code: PCC-CS392

Design (16x8b) memory using (4x8b)RAM

* THEORY

The memory blocks can be cascaded to implement larger blocks. There are different Control signals in RAM and FIFO blocks to control the cascading procedure. These signals are WE, RE and DEPTH. However, the variable aspect ratio of memory Blocks allows cascading in various configurations. The implementation of larger memory blocks can be categorized by two approaches: cascading in depth or width. In this Section we will discuss the difference between them as well as implementation of the two configurations. Cascading in depth means that all the building blocks have the same read and write width as the required memory block, but the address bus width of the required large memory block is larger than the address bus width of each Building block. For example, a 512x18 RAM block can be implemented by cascading two 256x18 RAM blocks, On the other hand, with width cascading the width of the Memory block address bus is equal to the address bus width of each building block. Each of the basic memory blocks is configured with the same depth as the required memory Block. For example, a 512x18 RAM block can be implemented with two 512x9 RAM blocks. In order to build larger memory blocks, memory cores can be cascaded both in depth and width if required. The preliminary characterization indicates that building large memory blocks by cascading in width shows better timing performance that the blocks implemented by cascading in depth. However, in some cases the only way to Implement larger blocks is by cascading blocks in depth (e.g., implementation of an 8kx1). In those cases, the user should try to keep the number of the depth-cascaded blocks as low as possible to improve the timing performance.

* CIRCUIT DIAGRAM



* RESULT & CONCLUSION

We implement vertical cascading of RAM IC with the 4 x 8 RAM IC for increasing depth of the memory blocks.